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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,802	01/15/2004	Dae-Woong Kang	8750-042	6500

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,802	KANG ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29-36* is/are allowed.

6)☒ Claim(s) *22-28,37 and 38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on May 24, 2006.

Previously Indicated Allowable Subject Matter

The indicated allowability of claim 38 is withdrawn in view of the newly discovered reference(s) to Furuta (US 6,921,947 B2). Rejections based on the newly cited reference(s) follow.

Claim Objections

Claim 38 is objected to because of the following informalities: Claim 38 recites the limitation "the first step region" in line 13. There is insufficient antecedent basis for this limitation in the claim and appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 22, 23, 28, 37, and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Furuta et al. (US 6,921,947 B2).

In re claim 22, Furuta et al. shows (fig. 1) a semiconductor device, comprising: a semiconductor substrate having a low voltage region (thin film portion BR) and a high voltage region (thick film portion AR); a first isolation layer (2 on the right) formed in the low voltage region and defining a first active region (5B); a second isolation layer (2 on the left) formed in the high voltage region and defining a second active region (5A); a low voltage gate insulation (GX2) layer formed on the first active region; and a high voltage gate insulation layer (GX1) formed on the second active region and having a greater thickness than the low voltage gate insulation layer. A step region is formed between the high voltage gate insulation layer and the second isolation layer wherein a bottom corner of the step region is spaced apart laterally from a vertical axis passing through an upper edge corner of the second active region (The step portion is the formed in the left side and center isolation regions 2. Each step portion is formed in the center of the isolations regions and faces the high voltage gate insulation layer GX1).

In re claim 23, Furuta shows (fig. 1) a low voltage gate electrode (GT2) formed on the low voltage gate insulation layer and disposed to cross over the first active region; and a high voltage gate electrode (GT1) formed on the high voltage gate insulation layer and disposed to cross over the second active region.

In re claim 28, Furuta shows in an alternate embodiment (fig. 14) that an edge region of the first isolation layer (2 on the right) is lower than a top surface of the low voltage gate insulation layer (GX2) because the isolation region has a recess portion that is formed below the top surface of the first active layer (5B).

In re claim 37, Furuta shows (fig. 1) that substantially the entire step region is spaced apart from the vertical axis passing through the edge corner of the second active region since the step region is formed in the center of the isolation layer and spaced away from the edge of the active region.

In re claim 38, Furuta et al. shows (fig. 1) a semiconductor device, comprising: a semiconductor substrate having a low voltage region (thin film portion BR) and a high voltage region (thick film portion AR); a first isolation layer (2 on the right) formed in the low voltage region and defining a first active region (5B); a second isolation layer (2 on the left) formed in the high voltage region and defining a second active region (5A); a low voltage gate insulation (GX2) layer formed on the first active region; and a high voltage gate insulation layer (GX1) formed on the second active region and having a greater thickness than the low voltage gate insulation layer. A step region is formed between the high voltage gate insulation layer and the second isolation layer wherein a distance between the bottom portion of the first step region (in isolation layer 2 on the left) and the bottom portion of the an adjacent step region (in isolation layer 2 in the center of the device) that is across the second active region from the first step region is greater that the width of the top surface of the second active region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24 –27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuta et al. (US 6,921,947 B2) as applied to claim 22 above, and further in view of Kim (US 6,642,105 B2).

In re claims 24 and 25, Furuta discloses (col. 1, lines 29-35) that devices having different driving voltages may comprise memory portions but does not specifically discloses that the low voltage region is a memory cell region or that the low voltage gate insulation layer is a tunnel oxide layer. Kim discloses (col. 2, lines 44-50) a device in which that the low voltage region is a memory cell region. Kim shows in (fig. 31b) that the low voltage gate insulation layer is a tunnel oxide layer. Forming the memory cell in this manner forms non-volatile memory devices having low power consumption. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Furuta by forming a memory cell array region in the low voltage region as taught by Kim to form a non-volatile memory device having low power consumption.

In re claim 26, Kim shows (fig. 32) that a control gate electrode (CG) is formed over the low voltage gate insulation layer (305b), the control gate electrode crossing over the first active region; a floating gate (FG) is interposed between the control gate electrode and the low voltage gate insulation layer; a main gate electrode formed on the high voltage gate insulation layer, the main gate electrode (313a) crossing over the second active region; a dummy gate electrode (317a) stacked on the main gate

electrode; and an inter-gate dielectric layer (315a) interposed between the floating gate and the control gate.

In re claim 27, Kim shows (fig. 32) that a thermal oxide (311) layer is interposed between the first isolation layer (309 right) and the semiconductor substrate, and between the second isolation layer (309 left) and the semiconductor substrate.

Response to Arguments

Applicant's arguments with respect to claims 22-28, 37, and 38 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claims 29-36 are allowed.

The following is an examiner's statement of reasons for allowance: the prior art references, alone or in combination, do not show a first active region having a protruded edge portion that extends above the top surface. The closest prior art reference, Chen et al. (US Pub. 2005/0199914 A1) shows (fig. 2H) a protruded edge portion (40), but does not show that the protruded edge portion extends above the top surface of the active region. Chen cannot be combined with Kim because Chen discloses a memory cell device having a floating gate formed in a trench in which the protruding edge injects electrons into the floating gate, whereas Kim only shows a trench isolation structure for separating active regions. The two devices are different and thus one of ordinary skill in the art could not look to Chen to find motivation for modifying or improving Kim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew E. Warren
August 6, 2006